Annexure A: Technical Specification (03 pages)

Supply and warranty of the items mentioned in the table below.

S. No.	Description	Quantity Required (Nos.)
1	**Programmable Logic Development Kit**	2
2	**Clock Generator Module**	1
3	**Clock Driver Module**	1
4	**Quadrature modulator evaluation board**	2
5	**Evaluation board for wide-band, low noise, fully differential amplifier**	2

Detailed technical specifications are given in the following table:

S. No.	Particular	Description
1.	**Programmable Logic Development Kit**	
	Features	**Specifications**
	FPGA device	Essential Features of high capacity SoC FPGA: • Logic density: 660k logic elements or more • Total Memory: 42600 kbit or more • Package / Case: FBGA-1517 or better • Number of user I/Os: 696 or more • Transceiver Data Rate: 17.4 Gbps or more • Number of Transceivers: 48, min. • Maximum Operating Temperature: + 100 °C • Minimum Operating Temperature: 0 °C • 18x19 bit multiplier: 3374 or more • Device should have embedded PCIe Hard IP and embedded Hard Memory controllers (2,400 Mbps DDR4, and 2,133 Mbps DDR3), Quad serial peripheral interface (QSPI) flash-controller, NAND flash controller, direct memory access (DMA)controller, Secure Digital/Multimedia Card (SD/MMC) controller. FPGA Development kit shall be able to support VHDL code optimized and compiled for ARRIA10. It should support 10/100/1000 Ethernet MAC as Soft IP Core.
	Communication Interface	• PCI Express (PCIe) Gen3x8 Expansion header. • Two 10/100/1000 SGMII Ethernet ports and one 10/100/1000 RGMII Ethernet port, two 10GbE small form factor pluggable (SFP) cages • One USB 2.0 port, USB On-The-Go (USB OTG) port • USB-UART port, DB-9 RS-232 Port, I2C port. • Dual FPGA mezzanine card (FMC) expansion headers for high speed serial communication with daughter board. One FMC loop-back card must be supplied. • Display port and serial digital interface (SDI) port
	Memory	• 1GB DDR4 HPS HILO memory card • NAND, QSPI, and SD/MICRO boot flash cards • 2GB DDR4 HILO memory card
	General requirements	• At least 4 user LEDs, 4 push button switches, 4 DIP Switches and Two-line character LCD display • Embedded FPGA Download Cable for hard processor system (HPS) or FPGA programming • Suitable Power Cables including AC adopters Cables

		and connectors for Programming the Board. • Soft copy of User manual, Technical reference Manual containing board schematic, layout file, Bill of Material and assembly information etc. should be supplied.
2.	**Clock Generator Module**	
	The evaluation board shall be a compact, easy-to-use platform for evaluating all the features of the clock attenuator IC. A VCXO shall be mounted on the evaluation board to provide a complete solution. All inputs and outputs shall be configured as differential on the evaluation board. The evaluation module shall offer a wide range of clock management and distribution features to simplify RF card clock tree designs. It shall be able to attenuate the incoming jitter of a primary system reference clock, such as a CPRI source, with the help of the narrow-band configured first PLL loop, which disciplines an external VCXO, and generate the low phase noise, high frequency clocks with the wider-band second PLL to drive data converter sample clock inputs. Evaluation module shall have Simple power connection using USB connection and on-board LDO voltage regulators, AC-coupled differential SMA connectors for 2 reference Inputs, 6 clock outputs and 1 VCXO output. It shall provide Microsoft Windows®–based evaluation software with simple graphical user interface with USB computer interface. It shall have On-board PLL loop filter and Status LEDs for diagnostic signals. Following are the minimum required specifications of the clock jitter attenuation/cleaner IC on the Evaluation board, bidder may quote for item with better specifications: • External VCO input to support up to 6000 MHz • Up to 14 LVDS, LVPECL, or CML type device clocks • Maximum output clock frequency up to 3200 MHz • JESD204B-compatible system reference (SYSREF) pulses • SPI-programmable phase noise vs. power consumption • Low rms jitter: 44 fs typical at 2457.6 MHz • Noise floor: −156 dBc/Hz at 2457.6 MHz • Low phase noise: −141.7 dBc/Hz or lower at 800 kHz, 983.04 MHz output • SYSREF valid interrupt to simplify JESD204B synchronization	
3.	**Clock Driver Module**	
	The Clock Driver Evaluation Board shall be a high performance, 3.2GHz, 14-Output Fanout clock buffer for the distribution of ultralow phase noise references for high speed data converters with either parallel or serial (JESD204B type) interfaces. Brief description of the module is as given below: The Evaluation Board shall provide 14 low noise and configurable outputs to offer flexibility in interfacing with many different components such as data converters, local oscillators, transmit/receive modules, field programmable gate arrays (FPGAs), and digital front-end ASICs. The Evaluation Board shall generate up to seven DCLK and SYSREF clock pairs per JESD204B interface. The Evaluation Board shall have independent flexible phase management of each of the 14 channels in such a way that All 14 channels feature both frequency and phase adjustment. The outputs shall also be programmable for 50 Ω or 100 Ω internal and external termination options. Clock Driver Evaluation Board shall have Simple power connection using USB connection and on-board low dropout (LDO) voltage regulator. It shall have SMA connectors for clock input, RF sync input, clock outputs. It shall have Easy access to digital input/output and diagnostic signals via input/output header (GPIO). Following are the minimum required specifications of the Buffer IC on the Evaluation board, bidder may quote for item with better specifications: • High performance, 3.2GHz, 14-Output Fanout clock buffer • Low additive jitter: <15 fs rms at 2457.6 MHz (12 kHz to 20 MHz) • Very low noise floor: -155.2 dBc/Hz at 983.04 MHz • Up to 14 LVDS, LVPECL, or CML type device clocks (DCLKs)	

	• JESD204B-compatible system reference (SYSREF) pulses • SPI-programmable adjustable noise floor vs. power consumption • Clock input to support up to 6 GHz
4.	**Quadrature modulator evaluation board**
	Evaluation board for 300 MHz to 4 GHz (or wider range), direct quadrature modulator like TRF3705. It must have the following features. • High Linearity: Output IP3: 30 dBm at 1850 MHz • Low Output Noise Floor: –160 dBm/Hz or lower • 78-dBc Single-Carrier WCDMA ACPR at –10 dBm Channel Power • Unadjusted Carrier Suppression: –40 dBm or better • Unadjusted Sideband Suppression: –45 dBc or better • Single Supply Operation • 1-bit Gain Step Control • Fast Power-Up/Power-Down
5.	**Evaluation board for wide-band, low noise, fully differential amplifier**
	Evaluation board for a wide-band (GBP: 8 GHz), low noise, fully differential amplifier like LMH5401. It must have the following features. • Gain Bandwidth Product (GBP): 8 GHz • Excellent Linearity Performance: DC to 2 GHz, G = 12 dB • Slew Rate: 17,500 V/µs • Low HD2, HD3 Distortion (1 VPP, 200 Ω, DE-DE, G = 12 dB): HD2 at -80 dBc or lower, HD3 at -77dBc or lower at 500 MHz • Low IMD2, IMD3 Distortion (2 VPP, 200 Ω, DE-DE, G = 12 dB): IMD2 at –80 dBc or lower, IMD3 at –83 dBc or lower at 500 MHz • Input Voltage Noise: 1.25 nV/√Hz or lower • Input Current Noise: 3.5 pA/√Hz or lower • Supports Single- and Dual-Supply Operation • Power-Down Feature

Terms and conditions

1. One-year warranty shall be provided for all the items.

2. Bidder must clearly specify the part number of the items they are offering. Bidder should submit the details (Technical specification, catalogues, user manuals etc.) of each of the item being offered with the quotations. Bidder should clearly mention compliance/Deviation if any from the tender specifications.

3. Acceptance Criteria:

   a. All the supplied items shall be new and sourced from OEM, refurbished items will be rejected. **The supplier must submit the Certificate of Conformance from the manufacturer of the items or original packing list/copy of delivery challan from the authorized distributors of the items from whom they have procured the same.**

   b. All the items shall meet the technical specifications as mentioned above.