| Specification of Desktop 8 Channel 14-bit 500MS/sec Digitizer | | |
|---|---|---|
| **GENERAL** | **Form Factor**<br>154x50x164 $mm^3$ (WxHxD) Desktop | Remarks |
| **ANALOG INPUT** | **Channels**<br>8 channels<br>single ended<br><br>**Impedance**<br>50 Ohm<br>**Connector**<br>MCX<br><br>**Full Scale Range**<br>0.5 or 2 Vpp<br>SW selectable<br>**Bandwidth**<br>250 MHz<br><br>**Offset**<br>Programmable DAC for DC offset adj.<br>Range: ± 1 V | |
| **DIGITAL CONVERSION** | **Resolution**<br>14 bits<br>**Sampling Rate**<br>500 MS/s<br>Simultaneously on each channel | |
| **ADC CLOCK GENERATION** | Clock source: internal/external<br>On-board PLL provides ADC sampling clock generation from an internal (50 MHz loc. oscillator) or external (front panel CLK-IN connector) reference | |
| **DIGITAL I/O** | **CLK-IN (AMP Modu II)**<br>AC coupled differential input clock<br>LVDS, ECL, PECL, LVPECL, CML<br>(single ended NIM/TTL available)<br>Jitter<100ppm<br><br>**TRG-IN (LEMO)**<br>External trigger input<br>NIM/TTL, Zin = 50 Ohm<br>**GPO (LEMO)**<br>General purpose output<br>NIM/TTL, Rt = 50 Ohm<br>**GPI (LEMO)**<br>General purpose input<br>NIM/TTL, Zin = 50 Ohm | |
| **MEMORY** | 5.12 MS/ch<br>Multi-Event Buffer with independent read and write access divisible into 1 ÷ 1024 buffers<br>Programmable event size and pre-post trigger | |

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| **TRIGGER** | **Trigger Source**<br>*Self-trigger*: channel over/under threshold for either Common or Individual (DPP only) trigger generation<br>*External-trigger*: Common by TRG-IN front panel connector<br>*Software-trigger*: Common by software command<br>**Trigger Propagation**<br>GPO digital output<br><br>**Trigger Time Stamp**<br>Waveform Recording: 31-bit counter, 16 ns resolution, 17 s range; 48-bit extension by firmware<br>DPP-PSD: 47-bit counter, 2 ns resolution, 78 h range; 10-bit and 2 ps fine time stamp with digital CFD<br>DPP-PHA: 47-bit counter, 2 ns resolution, 78 h range<br>DPP-DAW: 48-bit counter, 2 ns resolution, 156 h range<br>DPP-ZLEplus: 48-bit counter, 16 ns resolution, 625 h range | |
| **SYNCHRONIZATION** | **Clock Propagation**<br>One-to-many clock distribution from an external clock source on CLK-IN<br>Clock Cable delay compensation<br>**Acquisition Synchronization**<br>Sync Start/Stop through digital I/O (TRG-IN input, GPO output) External Trigger Time Stamp reset | |
| **ADC & MEMORY CONTROLLER FPGA** | Altera Cyclone EP4CE30 (one FPGA serves 4 channels) | |
| **COMMUNICATION INTERFACE** | **Optical Link**<br>up to 80 MB/s transfer rate<br>Daisy chainable: it is possible to connect up to 8/32 ADC modules to a single Optical Link Controller<br>**USB**<br>USB 2.0 compliant<br>Transfer rate up to 30 MB/s | |
| **FIRMWARE** | **Standard Firmware**<br>Digital Oscilloscope function<br><br>**DPP Firmware**<br>Special firmware for Digital Pulse Processing<br>DPP-Pluse Hight Analyse(PHA),<br>DPP-Pluse Shape Discriminator | |
| **Accessories** | | |
| **Cables** | LEMO 00 male to MCX male 1 m (8ch * 2=16) | |